OpenATE PA32IX

3U PXI Low Voltage Dynamic Digital PE Card

- 32 input / output channels, with static configuration
- 64 M of on-board vector memory per channel
- -0.5 ~ +5V VIH VIL per channel
  VTH per channel
- 50 MHz data rate
- 64M capture log memory
- Operates as a stand-alone card or with up to 16 boards in parallel
- API & Pattern Editor

Description

The PA32IX represents a new level of performance and capabilities for PXI-based digital instrumentation. Each card can function as a stand-alone digital subsystem or if required, multiple cards can be interconnected, supporting up to 512 bi-directional pins (16 boards). The PA32IX also supports deep pattern memory by offering 64 M of on-board vector memory with static per pin direction control and with test rates up to 50 MHz.

With new 64M capture memory, PA32IX can capture 32 channels data log .

Features

The PA32IX supports -0.5 ~ +5 VTH per channel ,VIH/ VIL per channel.

The PA32IX offers 1, 2 driver TG Edges, 1 strobe TG Edges, and four drive data formats are supported: RTZ (Return To Zero), RTO (Return To One), NRZ (Non Return To Zero), SBC (Surround By Complement) which can providing flexibility to create a variety of bus cycles and waveforms to test board and box level products

Compatibility

All OpenATE Interfaces PXI cards comply with the PXI Specification 2.0 (issued Aug. 2000)

Software

The PA32IX is supplied with API and Pattern Editor. Pattern Editor is a software tool that edits test patterns.

Application

- Digital Pattern Capture
- Digital Pattern Generation
- Hybrid and Digital IC Testing

OpenATE Inc.

The Open Solution for IC Tester

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Specifications

● **Pin Electronics**	
I/O Channels	32, per board resource
Test rate	50MHz
Input Level (Vih/ Vil)	-0.5 ~ +5V per channel
Output Level (Vth)	-0.5 ~ +5V per channels
Output Impedance	50 Ohm
● **Timing**	
Period Resolution	5nS
Pin TG Edge Resolution	5nS
Minimum Pulse Width	10nS
Driver TG Edges	2, per pin resource
Strobe TG Edges	1, per pin resource
● **Formater**	
Format Sets	1
RTZ, Return To Zero RTO, Return To One NRZ, Non Return To Zero SBC, Surround By Complement	
● **Environmental**	
Operating Temperature	0 ~ 50℃
Storage Temperature	-20 ~ 70℃

● **Logic Sequencer**	
Pattern Symbols	0, 1
LMSYNC to PXI Trigger Bus	For Sync With other Instruments
Ignore Fail By LM Address	YES
Vector Memory	64M(length) × 32(channels)
Log Memory	64M for capture log
● **Trigger**	
PXI_TRIG Bus	8
● **Physical Properties**	
Bus Interface	PXI
Dimensions	3U
Power Requirements	3.3V@3A, 5V@3A 12V@1A
System Clock	100MHz
Bus & Signals	8 PXI Trigger bus lines for parallel test
● **Software**	
●**Maximum boards in one system**	16
● **PXI Compliance**	
All OpenATE Interfaces PXI cards comply with the PXI Specification 2.0 (issued Aug, 2000)	

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